REMARKS

Favorable reconsideration of this Application as presently amended and in light of the following discussion is respectfully requested.

After entry of the foregoing Amendment, Claims 1-16 are currently pending in the present Application. Claims 1, 10 and 11 are amended by way of the present Amendment. Support for the amendment of these claims can be found at least in the specification at page 18, first paragraph. New Claims 12-16 have been added, support for which can be found at least in the specification at page 34, second paragraph. New Claim 12 is added to recite non-means-plus-function limitations. Thus, no new matter is added.

By way of summary, Claims 1, 3-7 and 9-11 stand rejected under 35 U.S.C. § 103 as being obvious over Robinett et al. (U.S. Publication No. 2002/0131443, hereinafter Robinett) in view of Okura et al. (U.S. Patent No. 5,297,139, hereinafter Okura); Claim 2 stands rejected under 35 U.S.C. § 103 as obvious over Robinett in view of Okura, and in further view of Baker (U.S. Patent No. 5,948,080).; Claim 8 stands rejected under 35 U.S.C. § 103 as obvious over Robinett in view of Okura, and in further view of Saito et al. (U.S. Patent No. 6,523,696, hereinafter Saito).

REJECTION UNDER 35 U.S.C. § 103

The Official Action has rejected Claims 1, 3-7 and 9-11 under 35 U.S.C. § 103 as being unpatentable over Robinett in view of Okura. The Official Action cites Robinett as disclosing the Applicant's invention with the exception of a detector for detecting the amount of data stored in a storage section. The Official Action cites Okura as disclosing this more detailed aspect of the Applicant's invention and states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the

cited references to arrive at the Applicant's claims. Applicant respectfully traverses the rejection.

Amended Claim 1 recites, *inter alia*, a data transfer apparatus including:

> ". . . storage means for storing data separately for each data flow which has been received from said first network and which is to be transferred to said second network, the second network having a non-coincident bus cycle with respect to the first network;
> detection means for detecting the amount of data stored in said storage means, for each data flow; and
> control means for controlling said data transferred to said second network in accordance with a detection result provided by said detection means."

By way of background, data transfer apparatuses are known for transferring isochronous data. For example, such data may include digital video (DV) transferred over an asynchronous transfer mode (ATM) network. When transferring such data between a sending node to a receiving node, it is often necessary to traverse several networks which may operate in accordance with a different clock signal. The lack of coincidence in the bus cycle of these disparate networks creates an undesirable difference in color and/or sound quality of the reproduced digital video signal.[1]

Due at least in part to the above deficiency in the art, the present invention is provided. With at least this object in mind, a brief comparison of the claimed invention, in view of the cited references, is believed to be in order.

Robinett describes a system and associated method of remultiplexing program-bearing data of an MPEG transport stream (TS). Primarily, the system is directed to MPEG-2 compliant transport streams which carry video programs.

Program clock reference (PCR) data is included in an extended data packet header of an MPEG transport stream, to represent a real-time clock count. If the associated packet is

[1] Application at pages 1-11.

moved in time within the transport stream, the PCR value of the moved packet will no longer be accurate. As remultiplexers have to recreate a new multiplex from a number of other multiplexes, it is inevitable that this process will result in packets being placed in different locations in the output stream then they had been in the input stream. In this case, the remultiplexer must edit the PCR values so that they reflect the values the clock counter would have had at the new location of the packet in the transport stream.[2] Likewise, the MPEG transport stream includes a program association table (PAT), which is transmitted at regular intervals and contains a list of all programs in the transport stream. Each program is further described by its own program map table (PMT) and the program ID (PID's) of the PMT's are contained in the PAT. Remultiplexers also edit the PAT and the PMT to correctly reflect the new transport stream content.

More specifically, adapters (110) function as a specialized synchronous interface and include direct memory access (DMA) control circuits (116). The DMA control circuit transfers transport packet data of the MPEG stream and descriptor data between the host memory (120) and the cache (114). The DMA control circuit enables continuous allocation of the descriptors and transport packet storage locations to incoming transport packets as they are received, i.e., from successive time slots.[3] In operation, an MPEG transport stream is received at a remultiplexer node (100) at one of a plurality of adapters (110). Each adapter is connected to a bus (130), which includes a host memory (120). By inputting a separate MPEG transport stream to a corresponding adaptor, the remultiplexer functions to integrate and re-time transport packets to produce an output remultiplexed bit stream.

Okura describes a data communication system for decreasing transmission delay. The system includes nodes (110) having a multiplexed transmission line (6) including data

[2] Robinett at paragraph 19.
[3] Robinett at paragraph 76.

structured in a plurality of time slots (7). A transmission line access section (5) provides packet data (8) to a receiving buffer (2). The quantity of data written and accumulated in the buffer is compared with a predetermined threshold for a predetermined period from a read-start point of time. When the quantity of accumulated data is the same as or less than the predetermined threshold, the buffer performs only writing of data from the communication transmission line. When the quantity of accumulated data is larger than the predetermined threshold, the buffer performs both a read and write operation with respect to the buffer at the same time during a predetermined period.[4]

Conversely, in an exemplary embodiment of the Applicant's invention, a data transfer apparatus is provided for transferring data between a first network and a second network. The second network has a non-coincident bus cycle with respect to the first network. An exemplary network system includes a digital video cassette recorded (11-1) operably linked to serial bus (12-1), which is in turn operably linked to a network, such as an asynchronous network (15-1). A data transfer apparatus (41-1) serves as a cycle master of the serial bus and the asynchronous network. Likewise, a digital video cassette recorder (19-2) is operably linked to a serial bus (18-2), which is in turn operably linked to a data transfer apparatus (42-2), which interfaces, for example, a further ansynchronous network (15-2). The asynchronous network (15-2) services as a cycle master of the serial bus (18-2) and has a bus cycle, which is non-coincident with respect to the asynchronous network (15-1).[5]

In operation, the data transfer apparatus (42-2) may receive digital video data transmitted from digital video cassette recorder (11-1) by way of serial network (12-1), asynchronous network (15-1) and asynchronous network (15-2). Upon receipt of such data from serial network (15-2), the data transfer apparatus (42-2) stores such data in intermediate

[4] Okura at column 4, lines 33-54.
[5] Application at Fig. 7; pages 16-17.

buffers such that different data flows are stored in different buffers. Detection circuitry is provided for detecting the amount of data stored in the memory for each data flow, and control circuitry manages the transfer of data to the second network in accordance with a detection result of the detection circuitry. In this way, timing differences in the data caused by the non-coincident bus cycles of the first and second network can be accounted for to eliminate undesirable artifacts in the reproduced digital video.[6]

As Robinett discloses a remultiplexing of MPEG streams, including adjustments to the PCR data, there is no disclosure or suggestion of the adjustment of a time stamp based upon the detected state of non-coincident bus cycles.

Neither Robinett, alone or in combination with Okura, disclose or suggest transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network, wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles, as recited in amended Claim 1 or any claim depending therefrom. Likewise, as independent Claims 10 and 11 recite substantially the same limitations discussed above, these claims, as well as any claims depending therefrom, are allowable at least for the same reasons.

Accordingly, Applicant respectfully requests that the rejection of Claim 1, 3-7 and 9-11 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claim 2 under 35 U.S.C. § 103 as being unpatentable over the combination of Robinett in view of Okura, and in further view of Baker. The Official Action states that Robinett and Okura disclose all the Applicant's claim limitations with the exception of an IEEE-1394 serial bus. The Official Action cites Baker as teaching

[6] Application at page 26, second full paragraph, 2 paragraph bridging pages 33 and 34.

this more detailed aspect of the Applicant's invention and states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references for arriving at the Applicant's claims. Applicant respectfully traverses the rejection. As discussed above, Robinett, neither alone or in combination with Okura, disclose or suggest the Applicant's data transfer apparatus including transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles. Likewise, Baker does not remedy this deficiency, and therefore, none of the cited references, either alone or in combination, can properly be asserted as disclosing or suggesting Applicant's Claim 2, which includes the above distinguished limitations by virtue of its dependency. Therefore, the Official Action does not provide a *prima facie* case of obviousness with regard to this claim.

Accordingly, Applicant respectfully requests that the rejection of Claim 2 under 35 U.S.C. § 103 be withdrawn.

The Official Action has rejected Claim 8 under 35 U.S.C. § 103 as being unpatentable over the combination of Robinett and Okura, and in further view of Saito. The Official Action states that Robinett and Okura disclose all of the Applicant's claim limitations with the exception of a first network connected to another first network, which is not synchronous in terms of a network clock. The Official Action cites Saito as teaching this more detailed aspect of the Applicant's invention and states that it would have been obvious to one skilled in the art at the time the invention was made to combine the cited references for arriving at the Applicant's claims. Applicant respectfully traverses the rejection.

As discussed above, Robinett, neither alone or in combination with Okura, disclose or suggest the Applicant's data transfer apparatus, which includes transferring data between a first network and a second network, the second network having a non-coincident bus cycle with respect to the first network wherein a memory status is detected so that control circuitry can transfer data to the second network in accordance with the detection result to avoid timing anomalies caused by non-coincident bus cycles. Likewise, Saito does not remedy this deficiency; and. therefore, none of the cited references, either alone or in combination, can properly be asserted as disclosing or suggesting Applicant's Claim 8, which includes the above distinguished limitation by virtue of its dependency. Therefore, the Official Action does not provide a *prime facie* case of obviousness with regard to this claim.

Accordingly, Applicant respectfully requests that the rejection of Claim 8 under 35 U.S.C. § 103 be withdrawn.

NEW CLAIMS

New Claim 12 recites substantially similar limitations to those discussed above and is provided for presenting the Applicant's invention in a format which does not invoke 35 U.S.C. § 112, 6th paragraph (means-plus-function format). Accordingly, Applicant submits that new Claim 12 is likewise allowable.

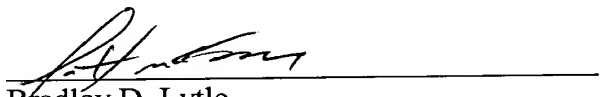
Claims 13-16 recite a further aspect of the Applicant's invention, wherein the detection result includes a determination as to a difference in a bus cycle time between the first and second networks. Applicant respectfully submits that this feature is not disclosed or suggested by the references of record.

CONCLUSION

Consequently, in view of the foregoing Amendment and remarks, it is respectfully submitted that the present Application, including Claims 1-16, is patently distinguished over the prior art, in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Bradley D. Lytle
Attorney of Record
Registration No. 40,073

Scott A. McKeown
Registration No. 42,866

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

BDL:SAM:ycs

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